REMARKS

Claims 1, 9, 15 and 21-35 are pending in the application. Claim 21 is amended herewith.

Claim 1 was rejected under 35 USC 103(a) as being unpatentable over KATSUKI et al. 5,581,767 in view of MAY et al. 6,414,368. That rejection is respectfully traversed.

Claim 1 recites at least four state control units that are directly interconnected to each other by respective dedicated event communication lines so that each of the at least four state control units is directly connected to all other ones of the state control units.

As recognized in the Official Action, KATSUKI fails to disclose communication between the processors using dedicated communication lines.

MAY is offered in an attempt to overcome the shortcomings of KATSUKI.

However, based on the disclosure of the references, one of ordinary skill would not have been motivated to combine the references in the first instance. Moreover, the references fail to disclose each of the recited features.

Column 7, lines 47-50 of KATSUKI disclose that direct connections have disadvantages. In order to overcome these disadvantages, KATSUKI uses his disclosed busses to provide communication between units.

As KATSUKI expressly teaches away from using a direct or dedicated communication line, it would not have been obvious to modify KATSUKI to use dedicated lines as suggested in the Official Action.

Moreover, even if one were motivated to make such a modification, the resultant modification would not result in that which is recited.

Figure 11 of MAY, reproduced below, shows an embodiment of MAY using dedicated connections 185, 186.

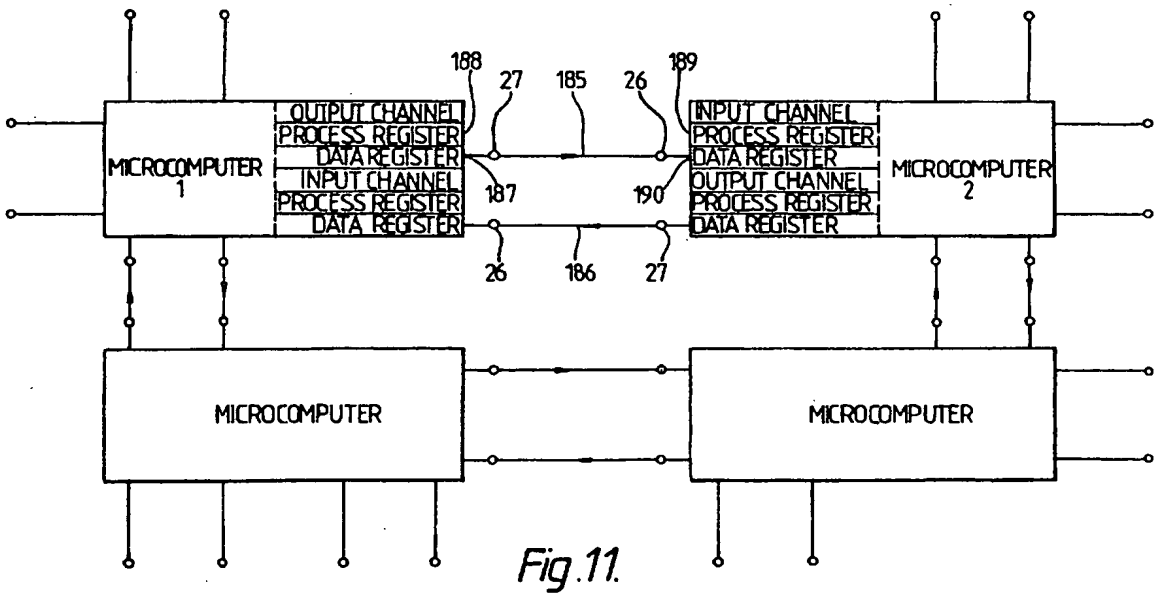

Fig.11.

As seen in the figure, of the four microcomputers shown, only the two immediately adjacent microcomputers are directly interconnected. MAY does not disclose that each of the at least four state control units is directly connected to all other ones of the state control units as recited.

The above-noted feature is missing from each of the references, is absent from the combination, and thus, would not have been obvious to one having ordinary skill in the art.

Claims 15, 21, 23-25, 30, 32, 33 and 35 were rejected under 35 USC 103(a) as unpatentable over KATSUKI in view of STOKES 3,537,074. That rejection is respectfully traversed.

The Official Action recognizes that KATSUKI does not disclose a multiplicity of processor elements is divided into element areas so that there is a state control unit for each element area and there is one state control unit for a plurality of processor elements.

STOKES is offered for this feature with the Official Action concluding that it would have been obvious to modify KATSUKI in view of STOKES to allow for a simpler design that increases flexibility and efficiency, because KATSUKI is not limited to a one-to-one embodiment.

However, this conclusion is untenable for at least the following reason.

KATSUKI at column 5, lines 32-37 disclose: "This invention is embodied in a bus structure ... comprising a processor ... and a control/memory section ... corresponding one-to-one to the aforementioned processor". In addition, each of the claims is directed to a one-to-one correspondence.

In view of the above, it is apparent that the entire disclosure of KATSUKI is explicitly limited to and thus, based on

the principal of operation of a one-to-one correspondence between a control unit and a processor.

Modifying KATSUKI in the manner suggested would change the principle of operation of KATSUKI. As one of ordinary skill in the art would not be motivated to change the principle of operation of KATSUKI, the teachings of the references are not sufficient to render the claims *prima facie* obvious.

Independent claim 21 recites that the multiplicity of processor elements is divided into a number of element areas corresponding to the number of state control units. The number of element areas being less than the multiplicity of processor elements.

Column 5, lines 35-37 of KATSUKI is offered for this feature.

However, this passage and all other passages of KATSUKI disclose a one-to-one correspondence between processor units and control units, not a correspondence between the element areas that make up the processor units and the control units.

As the recited number of element areas is less than the number of processor units, KATSUKI does not disclose that which is recited. STOKES is neither offered for this feature nor discloses such feature.

In addition, claim 21 is amended and recites a context, which is made up of the instruction codes of the multiplicity of processor elements, is switched for each operation cycle by a

state control unit in accordance with a computer program that has been installed in advance and the event data. Claim 21 further recites that the state transitions of the multiplicity of processors elements are done while changing a configuration of the multiplicity of processor elements.

In an array type processor as recited in claim 21, the context of the data path unit, which is made up of the instruction codes of the multiplicity of processor elements and the multiplicity of switch elements, is successively switched by a state control unit for each operation cycle. (see page 3, lines 4-7).

As recited in claim 21, the configuration of the data paths is changed by switching the instruction codes of the multiplicity of processor elements and the multiplicity of switches. Such switching the context of each operation cycle involves switching (changing) the configuration of the data paths (of the multiplicity of processor elements).

Furthermore, in the recited array processor, the context is switched not only by the computer program, but also by the event data.

In contrast, it is apparent that KATSUKI is directed to a bus architecture, which requires a bus protocol. KATSUKI is incapable of propagating the event data for each operation cycle, since KATSUKI requires operating on bus protocol. The bus

protocol of KATSUKI is a combination of a first bus for adjacent processors and a second bus for long-distance ones.

In view of the above, it is apparent that KATSUKI operates on a different premise than that which is recited. Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

Claims 23-25, 30, 32, 33 and 35 depend from claim 21 and further define the invention and are believed patentable at least or depending from an allowable independent claim.

Claims 22, 26-29, 31 and 34 were rejected under 35 USC 103(a) as unpatentable over KATSUKI in view of STOKES and further in view of MAY. That rejection is respectfully traversed.

MAY is only cited with respect to features of the dependent claims. MAY does not overcome the shortcomings of KATSUKI in view of STOKES set forth above with respect to claim 21. As claims 22, 26-29, 31 and 34 depend from claim 21 and further define the invention, claims 22, 26-29, 31 and 34 are believed patentable at least for depending from an allowable independent claim.

Claim 9 was rejected as unpatentable over KATSUKI in view of common art. That rejection is respectfully traversed.

The Official Action recognizes that KATSUKI fails to disclose a central control unit surrounded by a plurality of control units.

The position set forth in the Official Action is that the reference "Chip Layout Optimization Using Critical Path Weighting" discloses this feature and that it would have been obvious to modify MATSUKI in view of this reference.

However, this position is untenable because the above reference does not disclose that for which it is offered.

Although "Chip Layout Optimization Using Critical Path Weighting" discloses optimizing a routing area, nevertheless, this reference does not suggest that an optimal routing area includes a central control unit surrounded by the plurality of control units.

As each of the recited features is not disclosed by the references, *prima facie* obviousness has not been established.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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